

This Page Is Inserted by IFW Operations  
and is not a part of the Official Record

## **BEST AVAILABLE IMAGES**

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

**IMAGES ARE BEST AVAILABLE COPY.**

**As rescanning documents *will not* correct images,  
please do not report the images to the  
Image Problem Mailbox.**



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER OF PATENTS AND TRADEMARKS  
Washington, D.C. 20231  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/730,875	12/05/2000	Satoshi Ishida	2933SE-64-CON	9363

22442 7590 07/30/2002

SHERIDAN ROSS PC  
1560 BROADWAY  
SUITE 1200  
DENVER, CO 80202

EXAMINER
----------

LOKE, STEVEN HO YIN

ART UNIT	PAPER NUMBER
----------	--------------

2811

DATE MAILED: 07/30/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/730,875

Applicant(s)

ISHIDA ET AL.

Examiner

Steven Loke

Art Unit

2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 06 May 2002.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

Art Unit: 2811

1. Claim 1 is objected to because of the following informalities: line 1, "thing film transistor" is unclear whether it is being referred to "A thin film transistor"; line 4, "the insulator substrate an the gate electrode" is unclear whether it is being referred to "the insulator substrate and the gate electrode". Appropriate correction is required.

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsai et al. in view of Ono et al. (PTO-1449).

Tsai et al. discloses a thin film transistor in fig. 11. It comprises: an insulator substrate [71]; a gate electrode [72] located on the insulator substrate; a gate insulator film [73] provided above the insulator substrate and the gate electrode; and a polycrystalline silicon film [74, 176] located on the gate insulator film, the polycrystalline silicon film being formed by laser annealing step on a surface of an amorphous layer; the gate electrode having a center portion with a flat surface.

Tsai et al. differs from the claimed invention by not showing a pair of tapered end portions with inclined surfaces and an angle between each of the inclined surfaces of the pair of tapered end portions and a surface of the insulator substrate being set within a range of 5 to 40 degrees. ✓

Ono et al. shows a tapered end portion with inclined surface and an angle between the inclined surface of the tapered end portion and a surface of the insulator substrate being set to a range of 6 to 10 degrees (col. 18, lines 1-11).

Since both Tsai et al. and Ono et al. teach a thin film transistor with a bottom gate electrode, it would have been obvious to have the tapered end portion of the gate electrode of Ono et al. in each side of the gate electrode of Tsai et al. because it prevents the crack of the overlaying portion of the insulating film.

It is inherent that the combined device shows a uniform grain size of the polycrystalline silicon film formed above the center portion and the pair of tapered end portions of the gate electrode because the gate electrode having a center portion with a flat surface and a pair of tapered end portions with inclined surfaces, an angle between each of the inclined surfaces of the pair of tapered end portions and a surface of the insulator substrate being set within a range of 6 to 10 degrees.

Since the combined device shows the angle between each of the inclined surfaces of the pair of tapered end portions and a surface of the insulator substrate being set within a range of 6 to 10 degrees, it is inherent that a gate withstand voltage of the thin film transistor is prevented from increasing.

Since the combined device shows the angle between each of the inclined surfaces of the pair of tapered end portions and a surface of the insulator substrate being set within a range of 6 to 10 degrees, it is inherent that the laser beam is scanned on the surface of the amorphous silicon film such that a first portion of the amorphous silicon film above the gate electrode receives greater crystallization laser energy than a

Art Unit: 2811

second portion of the amorphous silicon film above the insulator substrate, and a third portion of the amorphous silicon film above the center portion receives greater crystallization laser energy than fourth portions of the amorphous silicon film above tapered end portions.

The process limitation of how the polycrystalline silicon film is formed has no patentable weight in claim drawn to structure. It is important to note that there are many ways to form a polycrystalline silicon film. Therefore, the phrases "formed by irradiating a laser beam on a surface of an amorphous silicon film to heat the amorphous film" and "the laser beam is scanned on the surface of the amorphous silicon film such that a first portion of the amorphous silicon film above the gate electrode receives greater crystallization laser energy than a second portion of the amorphous silicon film above the insulator substrate, and a third portion of the amorphous silicon film above the center portion receives greater crystallization laser energy than fourth portions of the amorphous silicon film above tapered end portions" are thus non-limiting.

4. Applicant's arguments filed 5/6/02 have been fully considered but they are not persuasive.

It is urged, in page 5 of the remarks, that Ono et al. does not teach or suggest setting the taper angle of the end portion within 5 degrees to 40 degrees in order to acquire a uniform grain size of the polycrystalline silicon film is acquired above the center portion and the pair of tapered end portions. However, the combined device of Tsai et al. and Ono et al. shows a gate electrode includes a pair of tapered end portions each having an angle being set within a range of 6 to 10 degrees. Since the combined device shows

Art Unit: 2811

the polycrystalline silicon film being formed by irradiating a laser beam on a surface of an amorphous silicon film which formed on the gate electrode having a center portion with a flat surface and a pair of tapered end portions each having an angle being set within a range of 6 to 10 degrees, it is inherent that a uniform grain size of the polycrystalline silicon film is acquired above the center portion and the pair of tapered end portions.

It is also urged, in pages 5-6 of the remarks, that Ono et al. never discloses the laser beam is scanned on the surface of the amorphous silicon film such that a first portion of the amorphous silicon film above the gate electrode receives greater crystallization laser energy than a second portion of the amorphous silicon film above the insulator substrate, and a third portion of the amorphous silicon film above the center portion receives greater crystallization laser energy than fourth portions of the amorphous silicon film above tapered end portions. Since the combined device shows the angle between each of the inclined surfaces of the pair of tapered end portions and a surface of the insulator substrate being set within a range of 6 to 10 degrees, it is inherent that the laser beam is scanned on the surface of the amorphous silicon film such that a first portion of the amorphous silicon film above the gate electrode receives greater crystallization laser energy than a second portion of the amorphous silicon film above the insulator substrate, and a third portion of the amorphous silicon film above the center portion receives greater crystallization laser energy than fourth portions of the amorphous silicon film above tapered end portions. In addition, the process limitation of

how the polycrystalline silicon film is formed has no patentable weight in claim drawn to structure (See the rejection of claim 1).

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (703) 308-4920. The examiner can normally be reached on 7:50 am to 5:20 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.



Application/Control Number: 09/730,875  
Art Unit: 2811

Page 7

sl  
July 28, 2002

Steven Loke  
Primary Examiner

A handwritten signature in cursive script that reads "Steven Loke". The signature is written in dark ink and is positioned below the printed name and title.